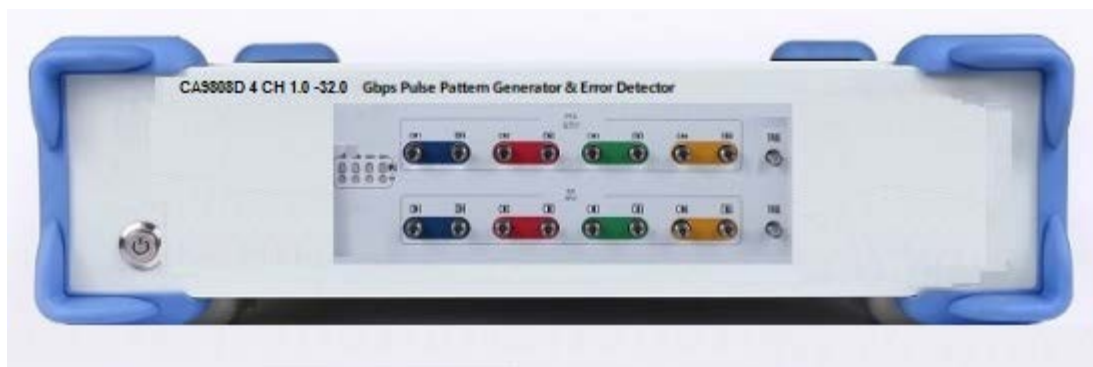


CA9808D 4 Channel 1.0 ~ 32.0 Gb/s Pulse Pattern Generator and Error Detector

Technical Specification V1.00

Feb, 2020



 UC INSTRUMENTS CORP.

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CA9808D 4 Channel 1.0 ~ 32.0 Gb/s Pulse Pattern Generator and Error Detector

(Ver 1.00)

The UC INSTRUEMNTS CA9808C 4 Channel 1.0 ~ 32.0 Gb/s pulse pattern generator and error detector is a high performance, flexible and cost effective four channel Pulse Pattern Generator and Error Detector that can operate from 1.0 Gb/s to 32.0 Gb/s each Channel. 4 channel 32.0 Gb/s make it total up to over more than 120 Gb/s testing capacity. It is also a standalone Bit Error Rate test solution that incorporates an internal full rate clock synthesizer.

Its small size allows it to be placed close to the Device Under Test (DUT), it can also be placed further away using the TX driver pre and post emphasis controls features to compensate for cable and interconnect losses. It also has a non destructive, integrated eye outline capture feature along with a quick eye height and width measurement capability.

The CA9808D was designed to characterize high speed digital links during the engineering, manufacturing or installation phases of a project. Such applications could include the testing of IC's, optical components, transceivers, copper cables, back planes and interconnects. The CA9808D can be used for compliance testing of Ethernet, Fiber Channel, Data-com, Infiniband, PCIE, SONET and proprietary link standards.

Features

- Four channel NRZ 1~32Gbps PPG and 1~32 Gbps ED
- Typical JRMS of 1 ps and JPP of 6 ps
- PRBS 2⁷, 9, 15, 23, 31
- Eye monitor
- Internal clock synthesizer
- PPM offset control
- Adjustable clock output
- External clock input
- TX level 100 to 1000 mV PPDIFF
- Pre and Post cursor emphasis (6 dB)
- TX squelch
- TX and RX polarity inversion
- Loss of signal indicator
- Programmable clock fixed pattern
- Burst error insertion
- USB 2.0 controlled
- API command set
- Stand alone configuration available
- Small size *377mm W×91mm H×460mmD*

Applications

- Multi-lane serial data channels signal integrity characteristic
- 100G/200G CFP2, CFP4, QSFP28 line cards
- Active Optical Cable (AOC), Direct Attach Cable (DAC)
- Electro-optical Transceiver Testing
- Design Validation Test (DVT) of Telecom / Data-com, Components, Modules and Systems
- High-Speed SerDes Testing & Characterization
- Installation and Maintenance Test of Network Equipment
- Testing of optical transceiver modules (SFP+, XFP, X2, Xenpak, XPAK), transponders, linecards, and subsystems
- Testing of opto-electronic components and devices (TOSA, ROSA, lasers, etc...)
- Testing of Gb/s ICs, PCBs, electronic modules, subsystems, and systems
- Serial bus and high-speed backplane design
- Installation testing and troubleshooting in optical transport networks
- Can be used for compliance testing of Ethernet, Fiber Channel, Infiniband, PCIE, SONET and proprietary link standards

Specification

TX Specification

Output Port Adaptor	2.92 mm Female
Standard Output Channel Clock Frequency	0.5GHz - 16GHz
Standard NRZ Output Pattern Rate	1.0 Gbps – 32.0 Gbps
Reference Clock Input	50MHz to 400MHz, single Channel 600mV±200mV@50Ω
Random Jitter	≤10mUI RMS, ≤300fs@28Gbps with real- time scope
Total Jitter	≤0.30UI
(Duty-free ratio) DCD	≤0.02UI
Deterministic Jitter	≤0.15UI
Rise/Fall Time	≤ 16ps(typ)@28Gbps
Single Ended Output	50mV-500mV(Adjustable)
Differential Out put	100mV-1000mV(Adjustable)
Polarity Reversal	Support
TEXQ Post-cursor 1	0-6dB 6 variable levels
TEXQ Post-cursor 2	0-6dB 6 variable levels
TEXQ Pre-cursor 1	0-6dB 6 variable levels
Coupling	AC
Clock Pattern	CLK_DIV2, CLK_DIV4, CLK_DIV8, CLKDIV_16
Random Pattern	PRBS7, PRBS9, PRBS15, PRBS23, PRBS31
Customerized Pattern	64bit Customer Setting
Output Rate Dynamically Adjustable	Support

RX Specification

Input Port Adaptor	2.92 mm Female
Data Rate	1.0 Gbps – 32.0 Gbps

Input Code	NRZ
Maximum Differential Voltage Input	1.2V
Input Sensitivity	40mV
Pattern Input	PRBS7, PRBS9, PRBS15, PRBS23, PRBS31 Error Detector
Data Sampling Self-Calibration	Sampling Alignment Support
Pattern Synchronization	Manual
Built-in CTLE	16 levels, automatic CTLE optimization or manual mode
Built-in DFE	8 levels, automatic DFE optimization or manual mode
Built-in CDR Input Rate	1.0 Gbps
Maximum Idle Code Length Input	120bit running length

BERT Specification

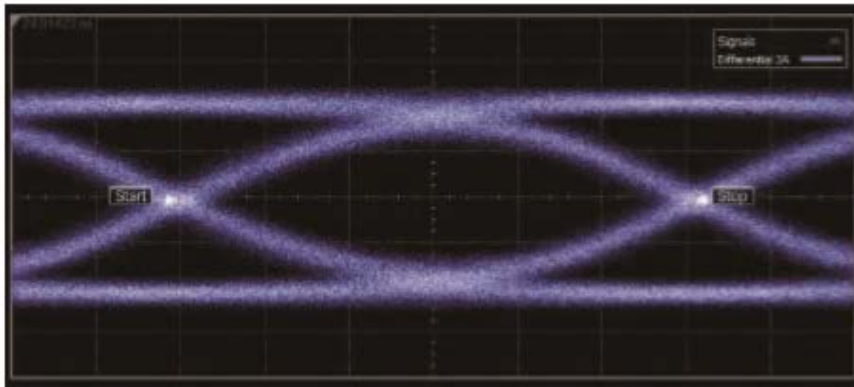
BERT Testing Function	Support. setting up waiting time or conditional bit error rate
BER Confidence	Supported
Eye Pattern Measurement	Eye Hight, eye width, Eye hight + Eye width(Eye open),

Data rate

CA9808D can address all common standard speeds via selectable bit rates between 1.0 Gb to 32.0Gbps.

Typical Eye Diagram

33 Gbps NRZ Eye Diagram

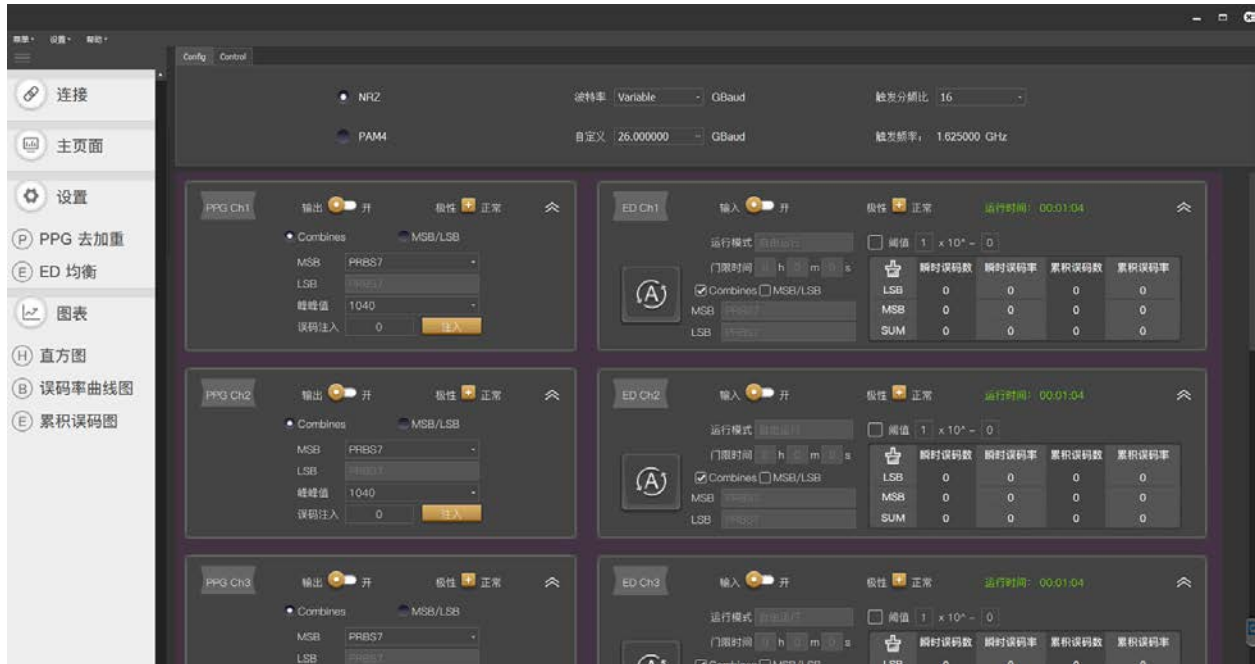


Parameter	Data
RJ	257fs
TJ@BER1E-15	7.93ps
DJ	4.49ps
PJ	1.72ps
DDJ	2.39ps
DCD	373.8fs
Eye-Width	25.92ps
Eye-Height	747mV

25.78 Gbps NRZ Eye Diagram



CA9808D Computer Control GUI



Typical CA9808D QSFP+ 4 X 28 Gb/s Testing System Configuration:

Contact Information

United States:

UC INSTRUMENTS CORP.

3652 Edison Way

Fremont, CA 94538

USA

Tel: 1-510-366-7353

Fax: 1-510-795-1795

www.ucinstruments.com

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