# CA9810 4/8 Channel 20.0 ~ 56.0 Gb/s PAM4

Bit Error Rate Tester

Technical Specification V3.0

July, 2018
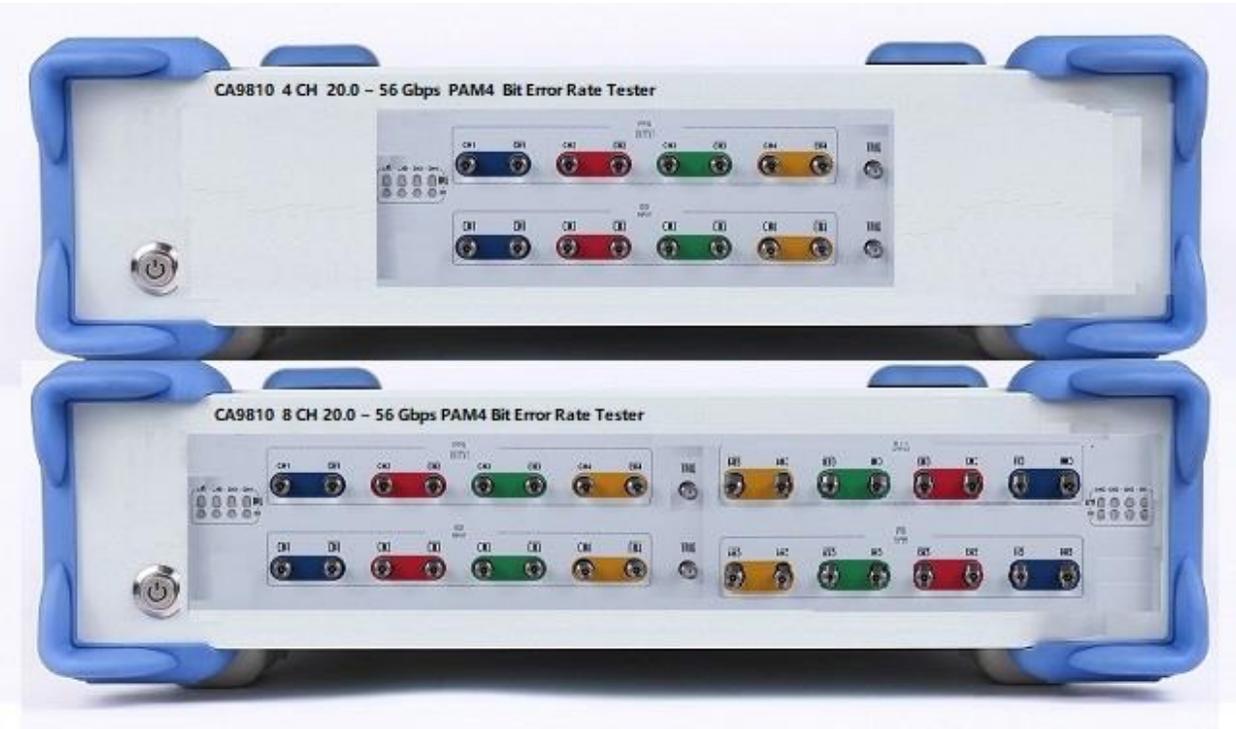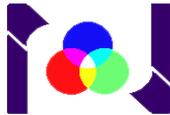
UC INSTRUMENTS CORP.

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CA9810 4/8 Channel 20.0 ~ 56.0 Gb/s PAM4

Bit Error Rate Tester

(Ver 3.00)

The UC INSTRUEMNTS CA9810 4/8 Channel 20.0 ~ 56.0 Gb/s PAM4 Bit Error Rate Tester is a high performance, flexible and cost effective four/eight channel PAM4 Bit Error Rate tester that can operate from 20.0 Gb/s to 56.0 Gb/s each Channel. 4/8 channel 56.0 Gb/s make it total up to over more than 240/480 Gb/s testing capacity.   It is also a standalone Bit Error Rate test solution that incorporates an internal full rate clock synthesizer.

Its small size allows it to be placed close to the Device Under Test (DUT), it can also be placed further away using the TX driver pre and post emphasis controls features to compensate for cable and interconnect losses. It also has a non destructive, integrated eye outline capture feature along with a quick eye height and width measurement capability.

The CA9808C was designed to characterize high speed digital links during the engineering, manufacturing or installation phases of a project. Such applications could include the testing of IC's,   optical components, transceivers, copper cables, back planes and interconnects. The CA9810 can be used for compliance testing of Ethernet, Fiber Channel, Data-com, Infiniband, PCIE, SONET and proprietary link standards.

Features

- Four/eight channel PAM4 signal generater

- 20.0 to 56.0 Gb/s data rate

- Typical JRMS of 1 ps and JPP of 6 ps

- PRBS 2^7, 9, 15, 23, 31

- Eye monitor

- Internal clock synthesizer

- PPM offset control

- Adjustable clock output

- External clock input

- TX level 200 to 1100 mV PPDIFF

- Pre and Post cursor emphasis (6 dB)

- Cross-Point Adjustment (35 to 65%)

- TX squelch

- TX and RX polarity inversion

- Loss of signal indicator

- Programmable clock fixed pattern

- Burst error insertion

- USB 2.0 controlled

- API command set

- Stand alone configuration available

- Small size *235mm W×45mm H×310mmD*

Applications

- Multi-lane serial data channels signal integrity characteristic
- 200G/400G CFP2, CFP4, QSFP28 PAM4 line cards
- Active Optical Cable (AOC), Direct Attach Cable (DAC)
- Electro-optical Transceiver Testing
- Design Validation Test (DVT) of Telecom / Data-com, Components, Modules and Systems
- High-Speed SerDes Testing & Characterization
- Installation and Maintenance Test of Network Equipment
- Testing of optical transceiver modules (SFP+, XFP, X2, Xenpak, XPAK), transponders, linecards, and subsystems
- Testing of opto-electronic components and devices (TOSA, ROSA, lasers, etc…)
- Testing of Gb/s ICs, PCBs, electronic modules, subsystems, and systems
- Serial bus and high-speed backplane design
- Installation testing and troubleshooting in optical transport networks
- Can be used forcompliance testing of Ethernet, Fiber Channel,
Infiniband, PCIE, SONET and proprietary link standards

Specification

TX Specification

Output Port Adaptor	2.92 mm Female
Output Channel Clock Frequency	0.5GHz - 17GHz
Standard NRZ Output Pattern Rate	1.0 Gbps – 34.0 Gbps
PAM4 Output Rate	20Gbps - 62 Gbps
Reference Clock Input	50MHz to 400MHz, single Channel 600mV±200mV@50Ω
Random Jitter	≤10mUI RMS, ≤300fs@28Gbps
Total Jitter	≤0.30UI
(Duty-free ratio) DCD	≤0.02UI
Deterministic Jitter	≤0.15UI
Rise/Fall Time	<= 14ps(typ)
Single Ended Output	11mV-600mV(Adjustable)
Differential Out put	22mV-1200mV(Adjustable)
Polarity Reversal	Support
Post-cursor 1	0-5.7 dB 20 variable levels
Post-cursor 2	0-2.1 dB 8 variable levels
Pre-cursor 1	0-3.9 dB 14 variable levels
Coupling	AC
Impedance Output	Choose from 100 ohm or 85 ohm difference
Clock Pattern	CLK, CLK_DIV2, CLK_DIV4, CLK_DIV8, CLKDIV_16, CLKDIV_32
PRBS Pattern	PRBS7, PRBS9, PRBS15, PRBS23, PRBS31
PAM4 Support Pattern	JP03A, JP03B, Linearity, PRBS7Q, PRBS9Q, PRBS10Q, PRBS13Q, PRBS15Q, PRBS23Q, PRBS31Q, QPRBS13
Customized Pattern	128bit Customer Setting
Dynamic Data Rate Change	Support

RX Specification

Input Port Adaptor	2.92 mm Female
Data Rate	1Gbps– 34GbpsNRZ, 20Gbps-56Gbps PAM4

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Input Data signal	NRZ or PAM4
Maximum Differential Voltage Input	1.2V
Input Sensitivity	25mV
Impedance Input	100 ohm or 85 ohm
Pattern Type	PRBS7, PRBS9, PRBS10, PRBS13, PRBS15, PRBS23, PRBS31,PRBS7Q, PRBS9Q, PRBS10Q, PRBS13Q, PRBS15Q, PRBS23Q, PRBS31Q Error Detector
Input equalization	Auto tuning or manual tuning
CDR input data rate	1Gbps– 34GbpsNRZ, 20Gbps-56Gbps PAM4
Data Input running length	120 bit running length
CDR recovered clock output	Support. Half-rate recovered clock output on CH2
CDR recovered data output	Support. Full-rate recovered data output on CH1

BERT Specification

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BERT Testing Function	Support. Time gating or infinite
BER Confidence	Supported
Eye contour	Eye Hight, eye width, Eye sum
Bathtub Curve	Horizontal timing, vertical amplitude

Data rate

CA9808C can address all common standard speeds via selectable bit rates between 1.0 Gb to 30.0Gbps.

## Typical PAM4 and Eye Diagram

PAM4 62 Gbps Eye Diagram (PRBS9)
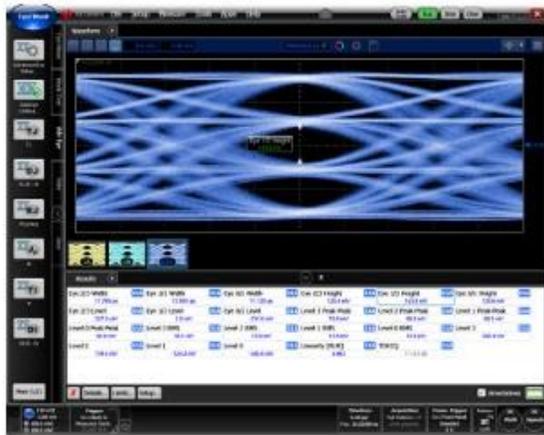
PAM4 53.125 Gbps Eye Diagram (PRBS9)
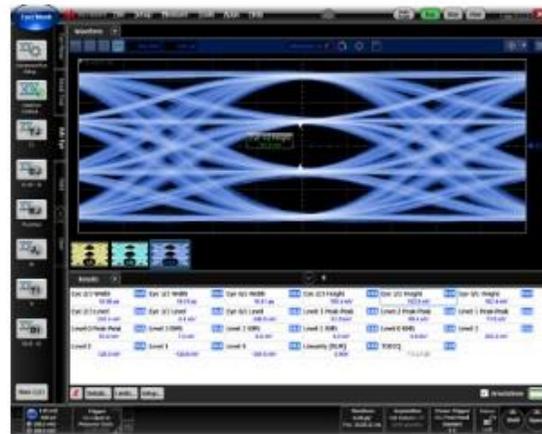
NRZ 28 Gbps Eye Diagram (PRBS9)
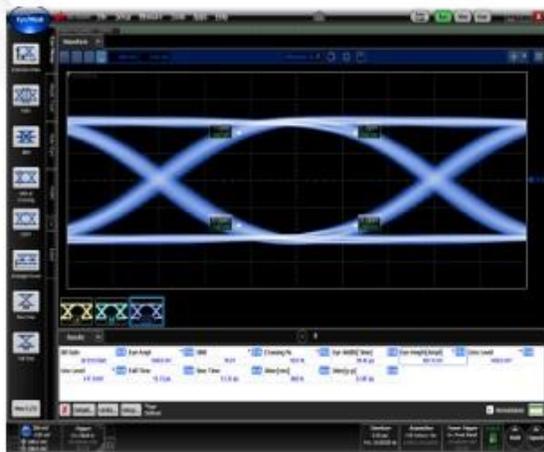
NRZ 25 Gbps Eye Diagram (PRBS9)
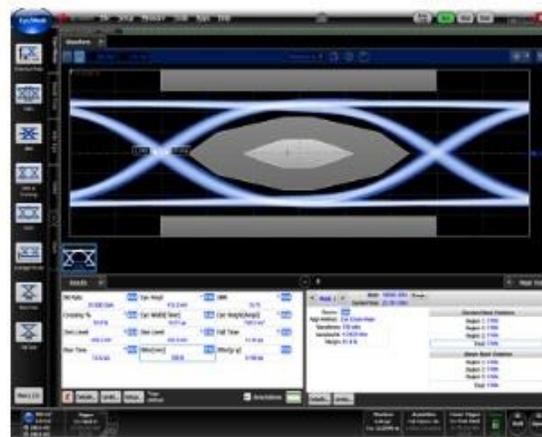
Built-in Eye Diagram and Bathtub Function

Built-in Eye Diagram Function
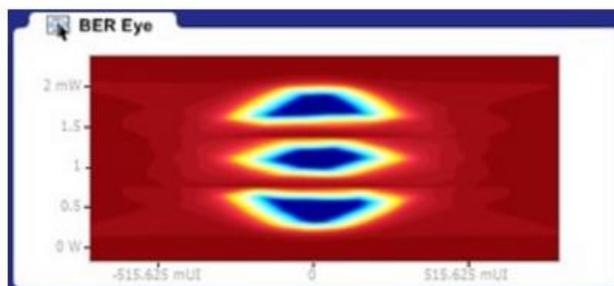
Built-in bathtub function
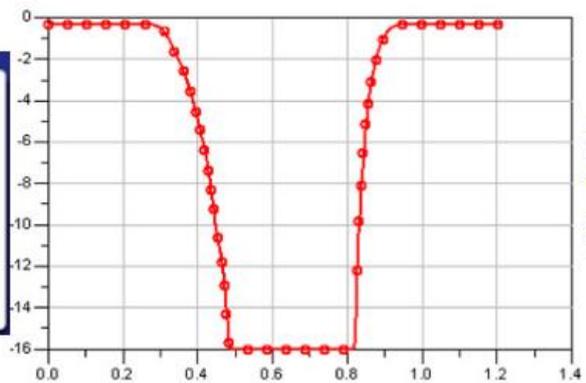
CA9810 PAM4 BERT Computer Control GUI
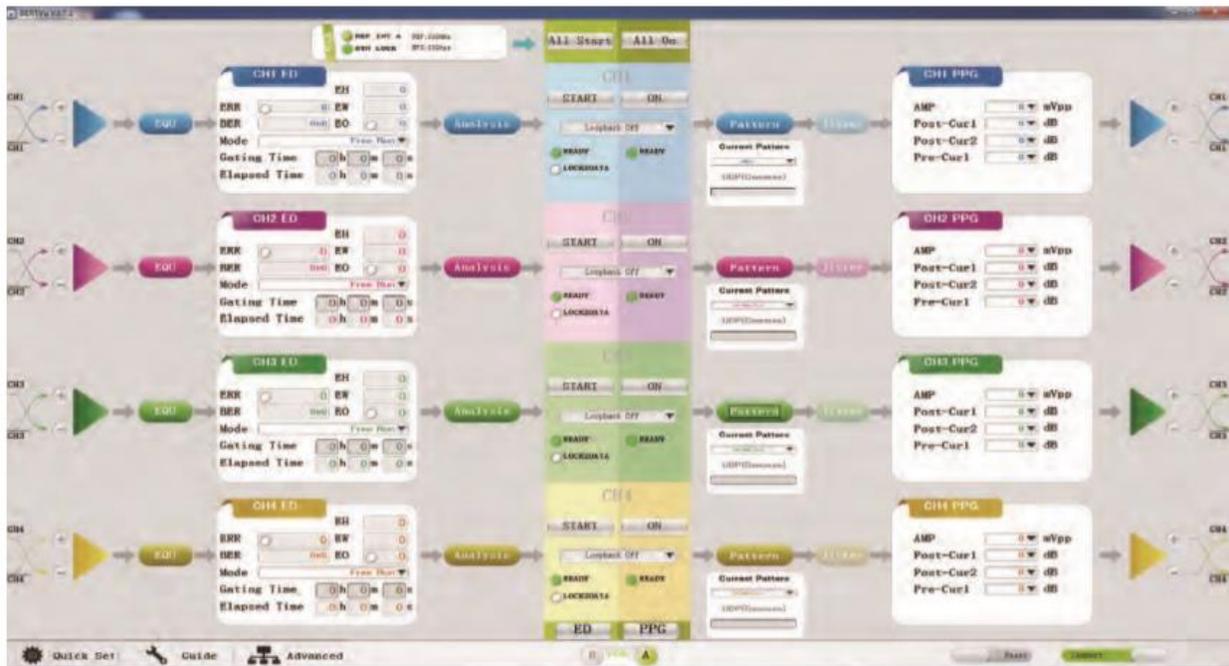
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Product specifications and descriptions in this documentation subject to change without notice.

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